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10/631,160	07/31/2003	James R. Peterson	200207081-1	7545

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EXAMINER	
PATEL, NIKETA I	

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
05/19/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/631,160	PETERSON ET AL.	
	Examiner	Art Unit	
	NIKETA I. PATEL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6 and 8-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/15/2008 have been fully considered but they are not persuasive. The applicant argues, in an essence, that the prior art of Malik (U.S. Patent Application Publication No.: 2004/0260908 A1) fails to teach the limitations of *a size of the first portion being responsive to the at least one characteristic of the first I/O device; determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device* as recited in claim 1 and similar limitations recited in other independent claims 6, 10, 15 and 19 [Remarks, pages 1-11.]

The examiner respectfully disagrees with these arguments. Malik (U.S. Patent Application Publication No.: 2004/0260908 A1) discloses the limitation of:

a. determining at least one characteristic of a first input/out (I/O) device **[figure 1, element 12]** that is coupled to a memory device interface **[figure 1, element 20]**,

b. the memory device interface being configured to enable data transfers between the first I/O device and a memory device **[figure 1, elements 22, 24, 26 (memory 1-3)]**;

c. buffering data corresponding to the first I/O device in a first portion **[figure 2, element 36]** of a buffer of the memory device interface **[figures 2, 3 – portion of pre-fetch buffer 30; bust lines 36, 38, 40, 42]**, a size of the first portion being

responsive to the at least one characteristic of the first I/O device **[paragraph 16 – "…The particular configuration of prefect buffer 30 is created by the prefetch control circuitry 32 in response to the Data Size signal and Burst Length signal, The Data Size signal determines the size of a single units of data within each burst line. The Burst Length signal determines the number of single units of data per burst line. FIG. 2, the Data Size signal selects a data size being a word in length. Other data sizes such as multiple words or a byte could be indicated by the Data Size signal. The Burst length signal allows the use of different types of bus masters to be implemented in data processing system 10. For example, if the first master 12 only supports bursts of eight words in length and the second bus master 14 supports bursts of four words in length, the prefetch buffer configuration of FIG. 2 will support both of these bus masters…" – i.e., the size of fist portion of a buffer (burst buffer size- eight words, four words) is determined based on characteristic of the fist I/O device (master 12)]**;

d. determining at least one characteristic of a second I/O device **[figure 1, element 14]** that is coupled to the memory device interface **[paragraph 16 – "…The particular configuration of prefect buffer 30 is created by the prefetch control circuitry 32 in response to the Data Size signal and Burst Length signal, The Data Size signal determines the size of a single units of data within each burst line. The Burst Length signal determines the number of single units of data per burst line. FIG. 2, the Data Size signal selects a**

data size being a word in length. Other data sizes such as multiple words or a byte could be indicated by the Data Size signal. The Burst length signal allows the use of different types of bus masters to be implemented in data processing system 10. For example, if the first master 12 only supports bursts of eight words in length and the second bus master 14 supports bursts of four words in length, the prefetch buffer configuration of FIG. 2 will support both of these bus masters…" – i.e., determining at least one characteristic (Data Size signal indicates the bust size supported) of a second I/O device (the master 14)]; and

e. buffering data corresponding to the second I/O device [**figure 1, element 14]** in a second portion of the buffer **[figure 2, element 40]**, a size of the second portion being responsive to the at least one characteristic of the second I/O device **[paragraph 16 – "…The particular configuration of prefect buffer 30 is created by the prefetch control circuitry 32 in response to the Data Size signal and Burst Length signal, The Data Size signal determines the size of a single units of data within each burst line. The Burst Length signal determines the number of single units of data per burst line. FIG. 2, the Data Size signal selects a data size being a word in length. Other data sizes such as multiple words or a byte could be indicated by the Data Size signal. The Burst length signal allows the use of different types of bus masters to be implemented in data processing system 10. For example, if the first master 12 only supports bursts of eight words in length and the second**

bus master 14 supports bursts of four words in length, the prefetch buffer configuration of FIG. 2 will support both of these bus masters…" – i.e., a size of the second portion (figure 2, element 40) being responsive to the at least one characteristic (Data Size signal indicates the bust size supported by the master 14, burst buffer size- eight words, four words) of the second I/O device (the master 14)].

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-6 and 8-19 rejected under 35 U.S.C. 102(e) as being anticipated by Malik et al. U.S. Patent Application Publication No.: 2004/0260908 A1 (hereinafter "*Malik*".)

4. **Referring to claim 1**, *Malik* teaches a method comprising: determining at least one characteristic of a first input/out (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the first I/O device and a memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being

responsive to the at least one characteristic of the first I/O device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; determining at least one characteristic of a second I/O device that is coupled to the memory device interface [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; and buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

5. **Referring to claim 2**, (Canceled).

6. **Referring to claim 3**, *Malik* teaches the method of claim 1, further comprising: receiving data from the first UO device via a first data transfer link [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; and receiving data from the second I/O device via a second data transfer link [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5.]

7. **Referring to claim 4**, *Malik* teaches the method of claim 1, further comprising: receiving a first data trait from the first I/O device; buffeting the first data unit in the first portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; and transferring the first data unit to the memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; receiving a second data unit from the second I/O device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; buffering the second data unit in the second portion of the buffer; and transferring the second data unit to the memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5.]

8. **Referring to claim 5**, *Malik* teaches the method of claim 1, wherein the at least one characteristic comprises at least one of: a rate at which the I/O device is able to read data from the memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; a rate at which the I/O device is able to write data to the memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; a bandwidth of a link coupled between the UO device and the memory device interface [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; a size of a data unit that the UO device reads from the memory device per read request [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; a size of a data unit that the I/O device writes to the memory device per write request [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; a tolerance that the UO device has for a delay by the memory device interface in fulfilling a write request [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; or a tolerance that the I./O device has for a delay by the memory device interface in fulfilling a read request [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

9. **Referring to claim 6**, *Malik* teaches a method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device, the method comprising: buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; buffering data received via a second data transfer link in a second portion of the buffer, a buffering capacity of the first portion being different than a buffering capacity of the second portion [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; and wherein the buffering capacity of

the first portion is responsive to at least one characteristic of a first I/O device that provides dam to the memory device interface via the first data transfer link, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

10. **Referring to claim 7**, (Canceled).

11. **Referring to claim 8**, *Malik* teaches the method of claim 6, further comprising: receiving a first data unit from the first I10 device via the first data transfer link [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; buffering the first data unit in the first portion of the buffer; transferring the first data unit to the memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; receiving a second data unit from the second I/O device via the second data transfer link; buffering the second data unit in the second portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; and transferring the second data unit to the memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

12. **Referring to claim 9**, *Malik* teaches the method of claim 6, further comprising: receiving a first data unit from the memory device; buffering the first data unit in the first portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; transferring the first data unit to the first UO device; receiving a second data unit from the memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; buffering the second data unit in the second portion of the buffer; and transferring the

second data unit to the second I/O device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

13. **Referring to claim 10**, *Malik* teaches a memory device interface that is configured to enable data transfers between an input/output (1/O) device, the memory device interface comprising: a buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first UO device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; and a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

14. **Referring to claim 11**, *Malik* teaches the memory device interface of claim 10, wherein the buffer comprises random access memory (RAM) [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

15. **Referring to claim 12**, *Malik* teaches the memory device interface of claim 10, wherein the first plurality of registers comprises: a first buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the first I/O device to be buffered in the first portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; and a second buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from

the second UO device to be buffered in the second portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

16. **Referring to claim 13**, *Malik* teaches the memory device interface of claim 12, wherein the value of the first buffer allocation counter is decremented responsive to a buffer allocation value being sent to the first UO device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

17. **Referring to claim 14**, *Malik* teaches the memory device interface of claim 13, wherein the value of the first buffer allocation counter is incremented responsive to data being read from the first portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

18. **Referring to claim 15**, *Malik* teaches a memory device interface comprising: a buffer; a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link; and a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link, a size of the first portion of the buffer being different than a size of the second portion of the buffer [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

19. **Referring to claim 16**, *Malik* teaches the memory device interface of claim 15, wherein the buffer comprises random access memory (RAM) [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

20. **Referring to claim 17**, *Malik* teaches the memory device interface of claim 15, wherein the first data transfer link is coupled to a first input/output (I/O) device, and the second data transfer link is coupled to a second I/O device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

21. **Referring to claim 18**, *Malik* teaches the memory device interface of claim 15, wherein the first plurality of registers comprises: a first buffer allocation counter that is configured to enable data received via the first data transfer link to be buffered in the first portion of the buffer; and a second buffer allocation counter that is configured to enable data received via the second data transfer link to be buffered in the second portion of the buffer.

22. **Referring to claim 19**, *Malik* teaches a system comprising: means for determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the UO device and a memory device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; means for buffering data corresponding to the first UO device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first FO device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5]; means for determining at least one characteristic of a second UO device that is coupled to the memory device interface; and means for buffeting data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at

least one characteristic of the second I/O device [see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5].

23. **Referring to claim 20**, (Canceled.)

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKETA I. PATEL whose telephone number is (571)272-4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272 4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Niketa I. Patel/
Primary Examiner, Art Unit 2181